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Lindsay

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(54) **METHOD AND APPARATUS FOR TESTING MEMORY DEVICES AND DISPLAYING RESULTS OF SUCH TESTS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: **Sep. 20, 2000**

Related U.S. Application Data

(63) Continuation of application No. 08/915,074, filed on Aug. 20, 1997, now Pat. No. 6,134,677, which is a continuation of application No. 08/567,069, filed on Dec. 4, 1995, now Pat. No. 5,720,031.

(51) **Int. Cl.**[7] **G06F 11/00**
(52) **U.S. Cl.** **714/42**
(58) **Field of Search** 714/42, 48, 57, 714/53, 46, 54, 423; 365/200, 201

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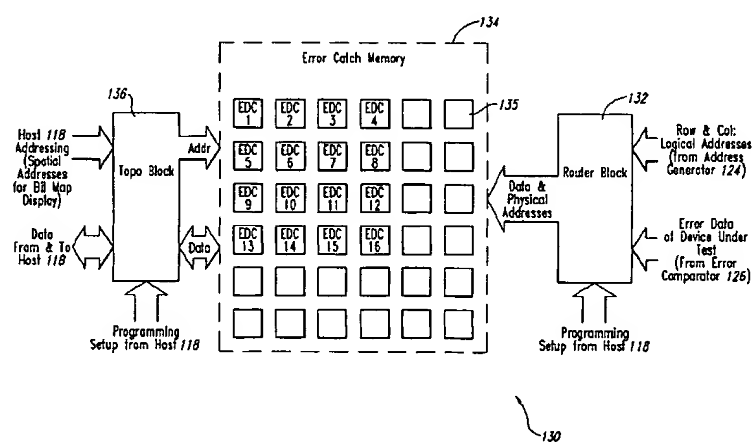
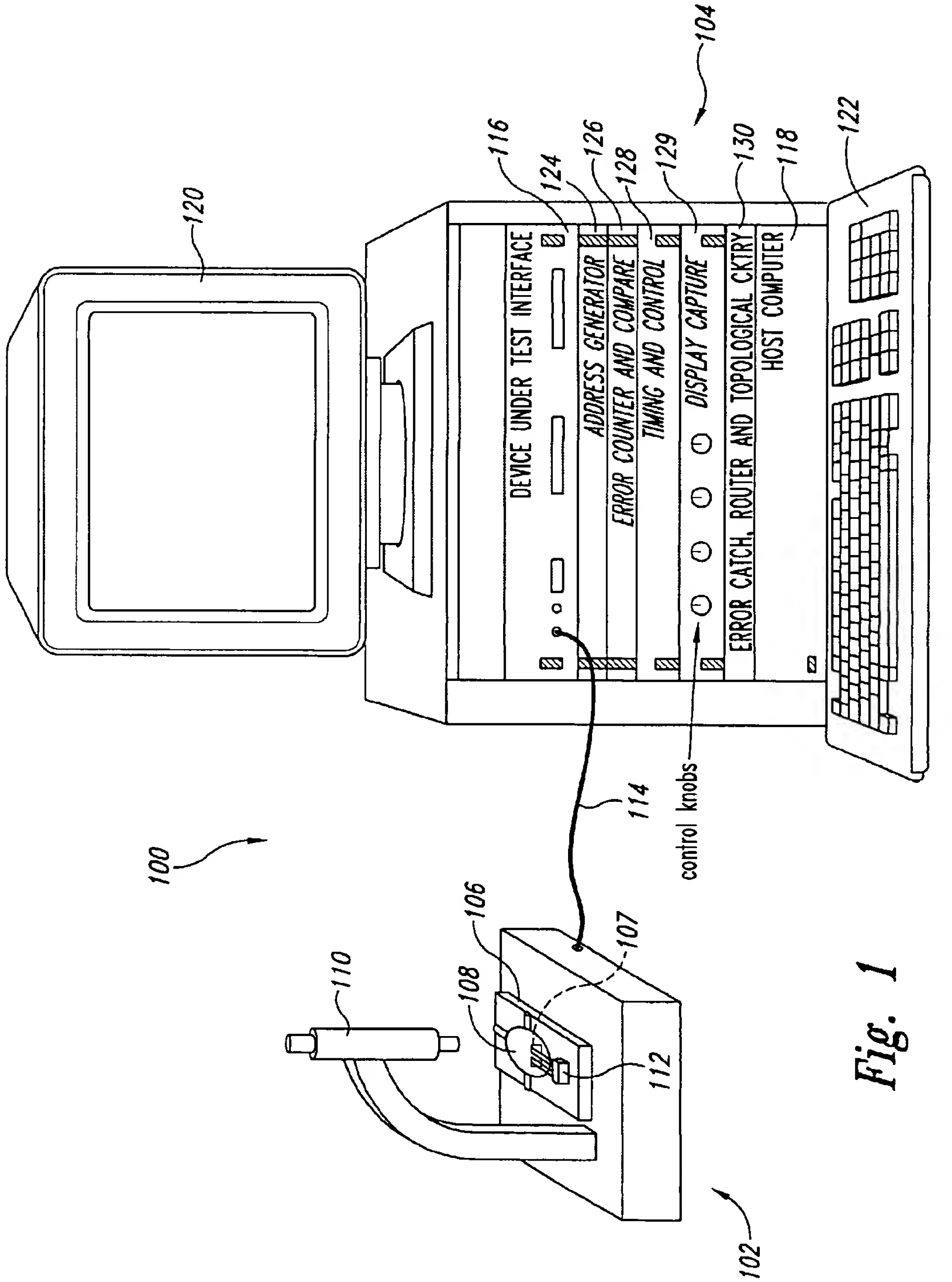
(57) **ABSTRACT**

An apparatus and method for testing a semiconductor device allows error data to be displayed, in real time, based on the physical locations of the errors on the semiconductor device. A mapping circuit includes a router circuit, an error catch memory, and a topological circuit. The router circuit converts logical addresses employed by the semiconductor device to physical addresses employed by the error catch memory so that error data is appropriately routed from locations in the semiconductor device to corresponding locations in the error catch memory. The topological circuit then converts the physical addresses of the error data in the error catch memory to spatial addresses for allowing a host computer to rapidly display such errors as a bit map display on a visual display device. The router and topological circuits are preferably field programmable gate arrays or programmable read only memories so that the host computer can reprogram them for different semiconductor devices to be tested.

29 Claims, 11 Drawing Sheets



06/23/2002, EAST Version: 1.03.0002



DEVICE UNDER TEST INTERFACE
ADDRESS GENERATOR
ERROR COUNTER AND COMPARE
TIMING AND CONTROL
DISPLAY CAPTURE
ERROR CATCH, ROUTER AND TOPOLOGICAL CKTRY
HOST COMPUTER
control knobs
100
102
104
106
107
108
110
112
114
116
118
120
122
124
126
128
129
130

Fig. 1

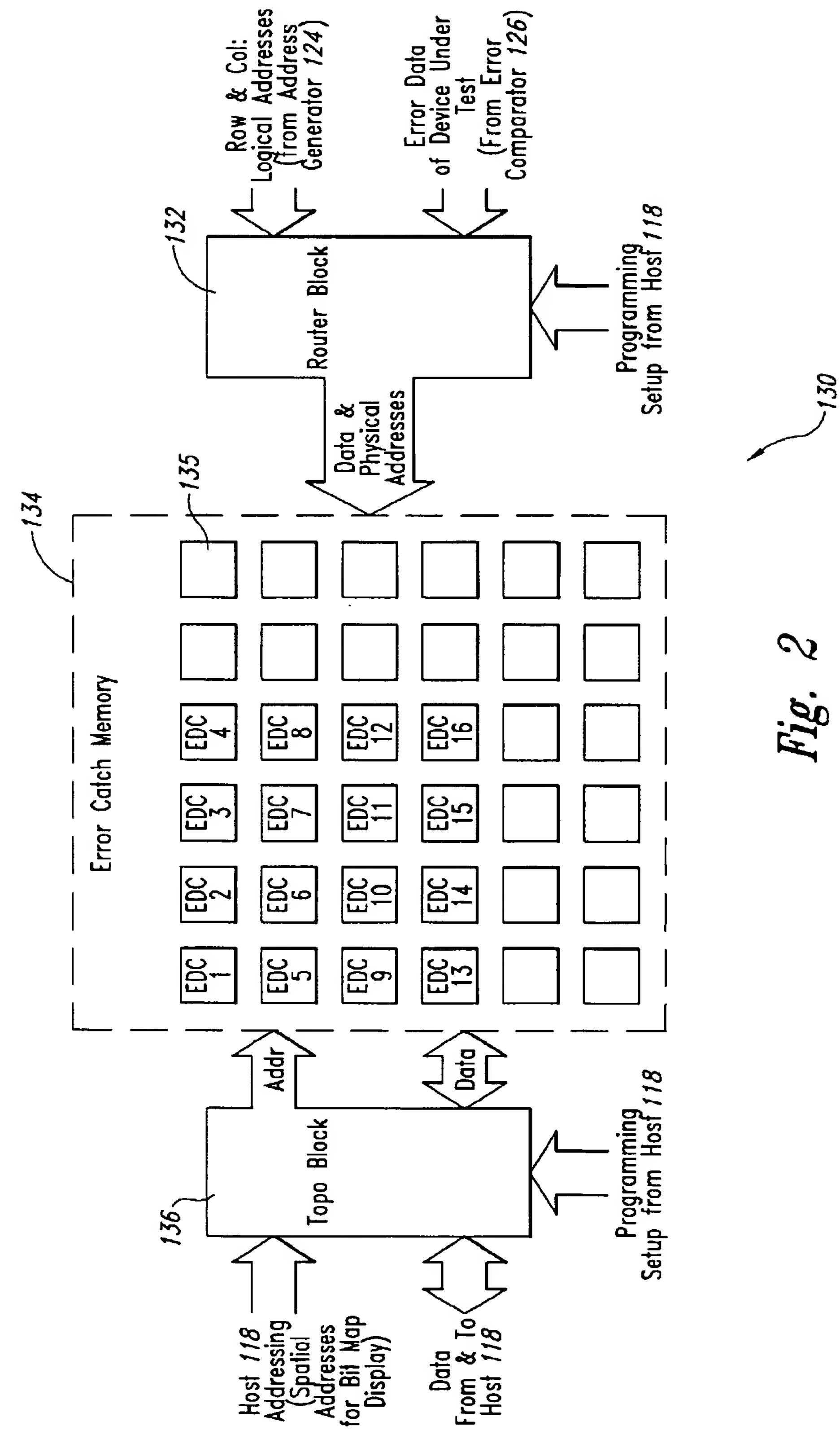

Row & Col: Logical Addresses (from Address Generator 124)
Error Data of Device Under Test (From Error Comparator 126)
132
Router Block
Programming Setup from Host 118
Data & Physical Addresses
130
134
135
Error Catch Memory
EDC 1
EDC 2
EDC 3
EDC 4
EDC 5
EDC 6
EDC 7
EDC 8
EDC 9
EDC 10
EDC 11
EDC 12
EDC 13
EDC 14
EDC 15
EDC 16
Addr
Data
136
Topo Block
Programming Setup from Host 118
Host 118 Addressing (Spatial Addresses for Bit Map Display)
Data From & To Host 118

Fig. 2

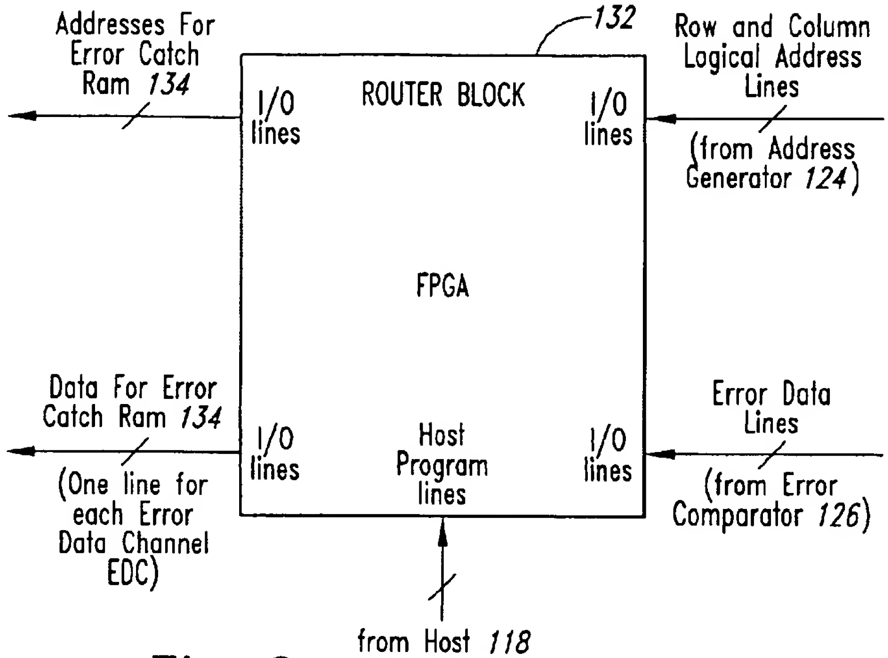

132
Addresses For Error Catch Ram 134
ROUTER BLOCK
I/O lines
I/O lines
Row and Column Logical Address Lines
(from Address Generator 124)
FPGA
Data For Error Catch Ram 134
(One line for each Error Data Channel EDC)
I/O lines
Host Program lines
I/O lines
Error Data Lines
(from Error Comparator 126)
from Host 118

Fig. 3

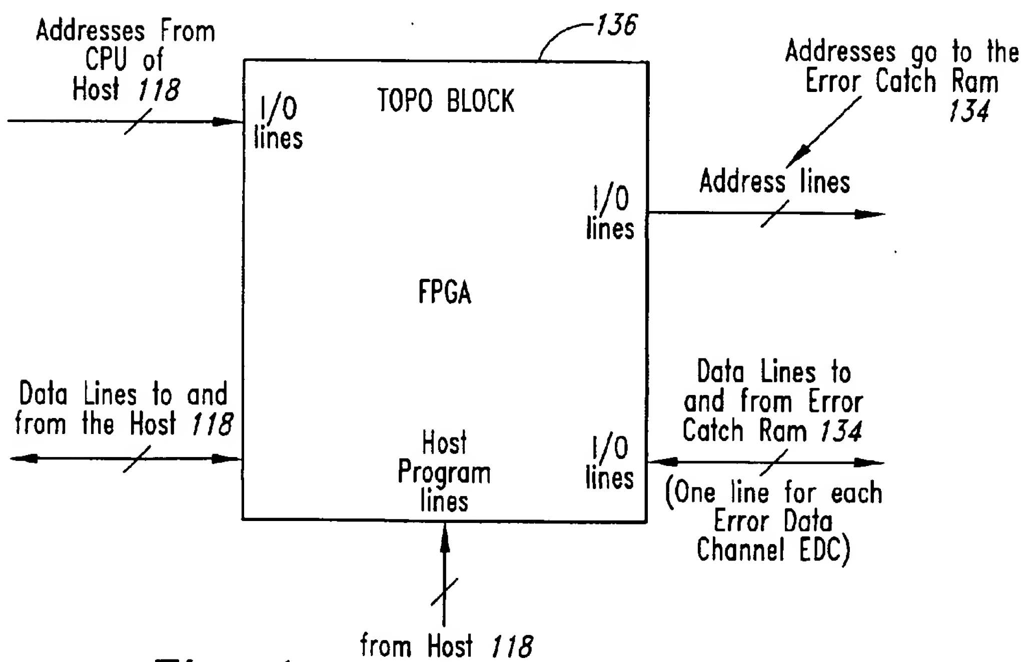

136
Addresses From CPU of Host 118
I/O lines
TOPO BLOCK
Addresses go to the Error Catch Ram 134
Address lines
I/O lines
FPGA
Data Lines to and from the Host 118
Host Program lines
I/O lines
Data Lines to and from Error Catch Ram 134
(One line for each Error Data Channel EDC)
from Host 118

Fig. 4

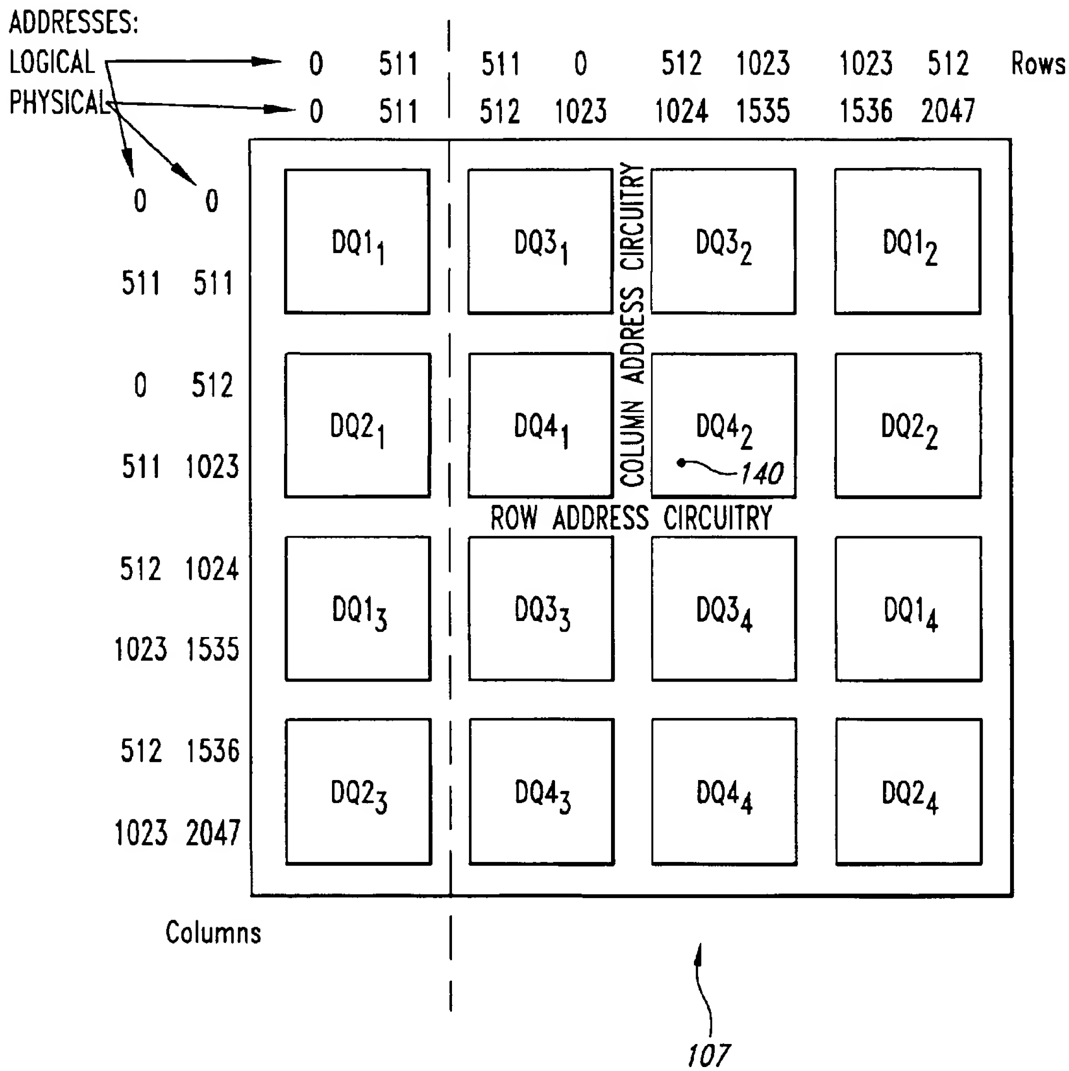

ADDRESSES:
LOGICAL
PHYSICAL
0 511 511 0 512 1023 1023 512 Rows
0 511 512 1023 1024 1535 1536 2047
0 0
511 511
0 512
511 1023
512 1024
1023 1535
512 1536
1023 2047
$DQ1_1$
$DQ3_1$
$DQ3_2$
$DQ1_2$
$DQ2_1$
$DQ4_1$
$DQ4_2$
$DQ2_2$
140
COLUMN ADDRESS CIRCUITRY
ROW ADDRESS CIRCUITRY
$DQ1_3$
$DQ3_3$
$DQ3_4$
$DQ1_4$
$DQ2_3$
$DQ4_3$
$DQ4_4$
$DQ2_4$
Columns
107

Fig. 5

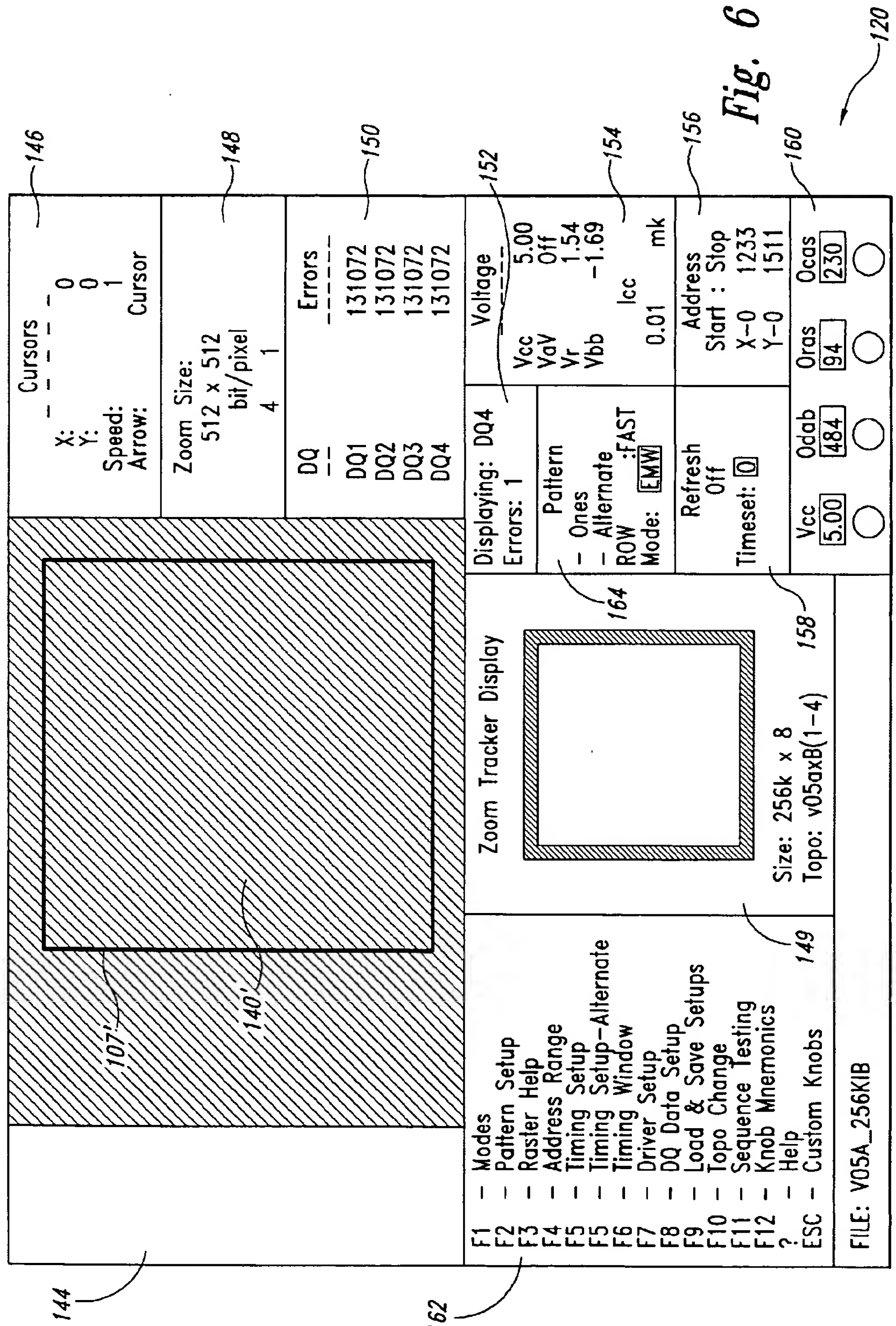

Cursors
X: 0
Y: 0
Speed: 1
Arrow: Cursor
Zoom Size:
512 x 512
bit/pixel
4 1
DQ
DQ1
DQ2
DQ3
DQ4
Errors
131072
131072
131072
131072
Voltage
Vcc 5.00
VaV Off
Vr 1.54
Vbb -1.69
Icc
0.01 mk
Displaying: DQ4
Errors: 1
Pattern
- Ones
- Alternate
ROW :FAST
Mode: EMW
Address
Start : Stop
X-0 1233
Y-0 1511
Refresh
Off
Timeset: 0
Vcc 5.00
Odab 484
Oras 94
Ocas 230
Zoom Tracker Display
Size: 256k x 8
Topo: v05axB(1-4)
F1 - Modes
F2 - Pattern Setup
F3 - Raster Help
F4 - Address Range
F5 - Timing Setup
F5 - Timing Setup-Alternate
F6 - Timing Window
F7 - Driver Setup
F8 - DQ Data Setup
F9 - Load & Save Setups
F10 - Topo Change
F11 - Sequence Testing
F12 - Knob Mnemonics
? - Help
ESC - Custom Knobs
FILE: V05A_256KIB
120
144
146
148
149
150
152
154
156
158
160
162
164
107'
140'

Fig. 6

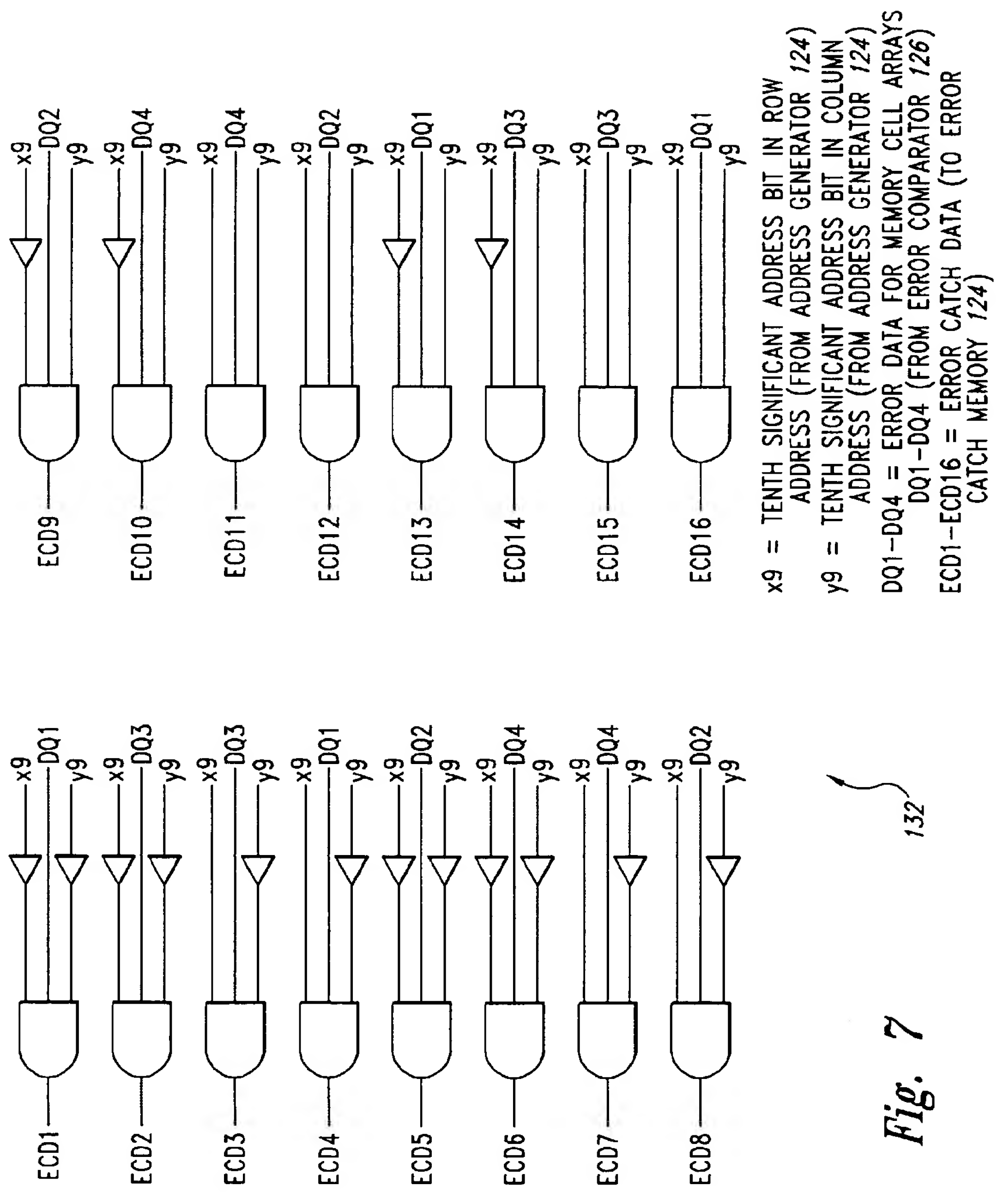

ECD1
ECD2
ECD3
ECD4
ECD5
ECD6
ECD7
ECD8
ECD9
ECD10
ECD11
ECD12
ECD13
ECD14
ECD15
ECD16
x9
y9
DQ1
DQ2
DQ3
DQ4
132
x9 = TENTH SIGNIFICANT ADDRESS BIT IN ROW ADDRESS (FROM ADDRESS GENERATOR 124)
y9 = TENTH SIGNIFICANT ADDRESS BIT IN COLUMN ADDRESS (FROM ADDRESS GENERATOR 124)
DQ1–DQ4 = ERROR DATA FOR MEMORY CELL ARRAYS DQ1–DQ4 (FROM ERROR COMPARATOR 126)
ECD1–ECD16 = ERROR CATCH DATA (TO ERROR CATCH MEMORY 124)

Fig. 7

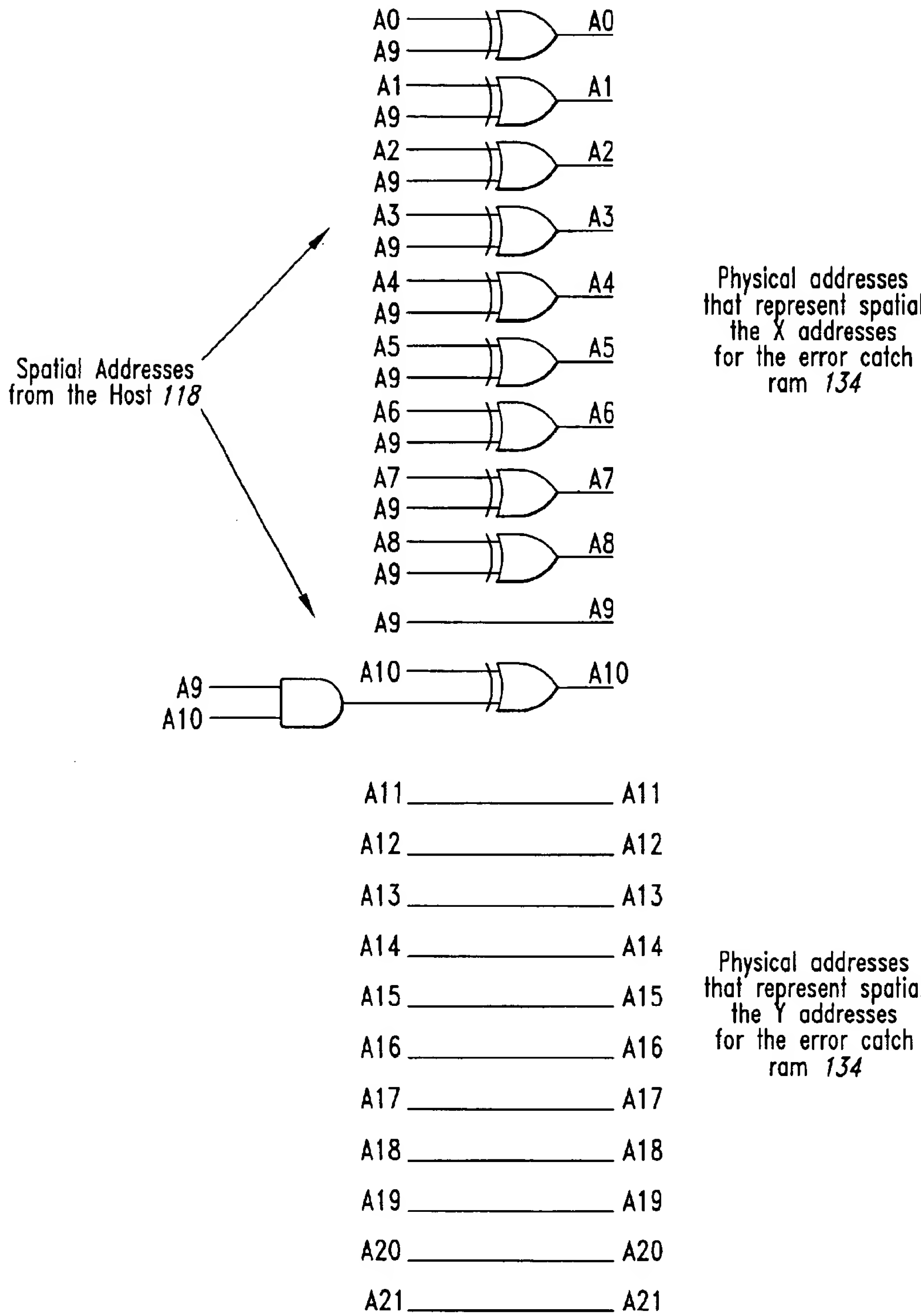
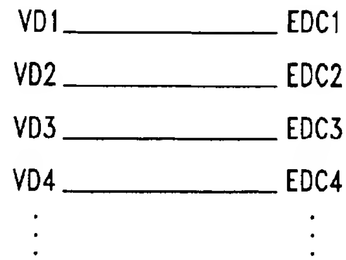
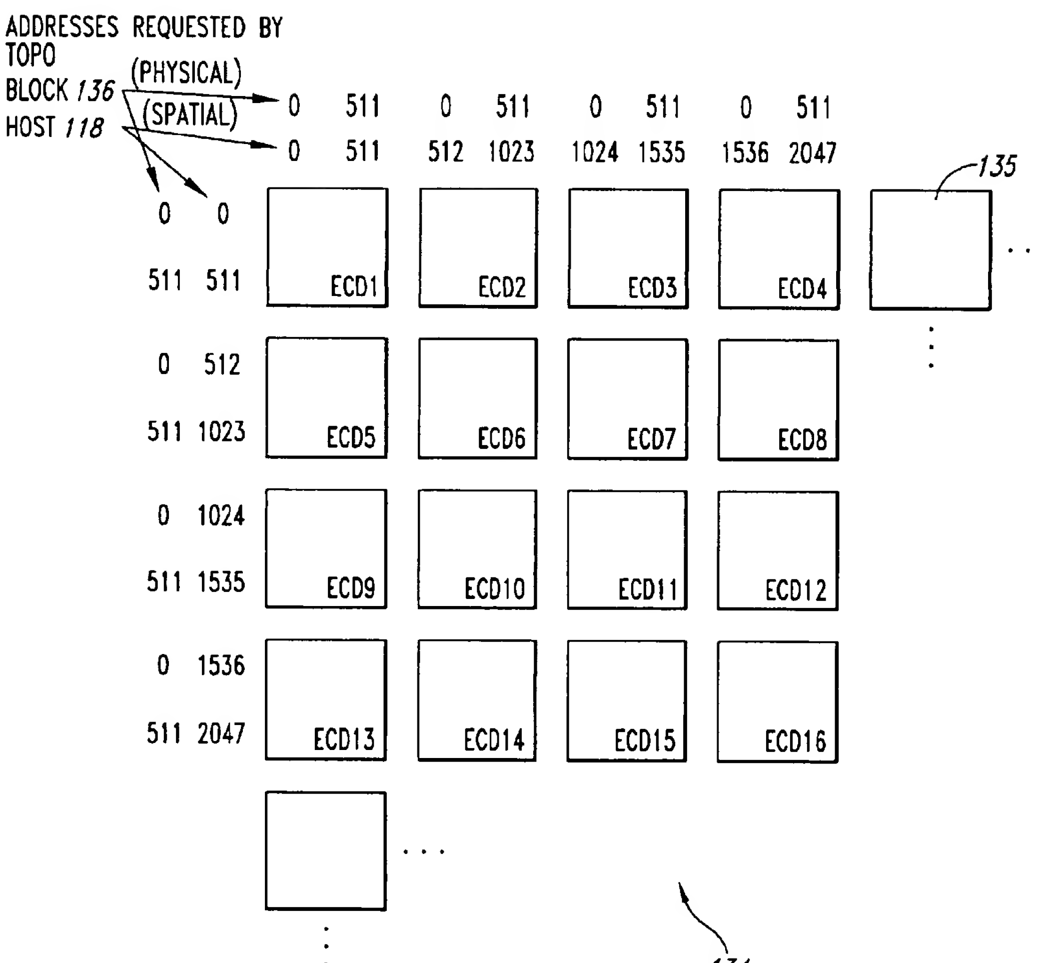

A0
A9
A0
A1
A9
A1
A2
A9
A2
A3
A9
A3
A4
A9
A4
A5
A9
A5
A6
A9
A6
A7
A9
A7
A8
A9
A8
A9
A9
A9
A10
A10
A10
A10
A11 A11
A12 A12
A13 A13
A14 A14
A15 A15
A16 A16
A17 A17
A18 A18
A19 A19
A20 A20
A21 A21
Spatial Addresses from the Host 118
Physical addresses that represent spatial the X addresses for the error catch ram 134
Physical addresses that represent spatial the Y addresses for the error catch ram 134

Fig. 8



VD1
EDC1
VD2
EDC2
VD3
EDC3
VD4
EDC4

Fig. 9



ADDRESSES REQUESTED BY
TOPO
BLOCK 136
HOST 118
(PHYSICAL)
(SPATIAL)
0 511 0 511 0 511 0 511
0 511 512 1023 1024 1535 1536 2047
135
0 0
511 511
ECD1
ECD2
ECD3
ECD4
0 512
511 1023
ECD5
ECD6
ECD7
ECD8
0 1024
511 1535
ECD9
ECD10
ECD11
ECD12
0 1536
511 2047
ECD13
ECD14
ECD15
ECD16
134

Fig. 10

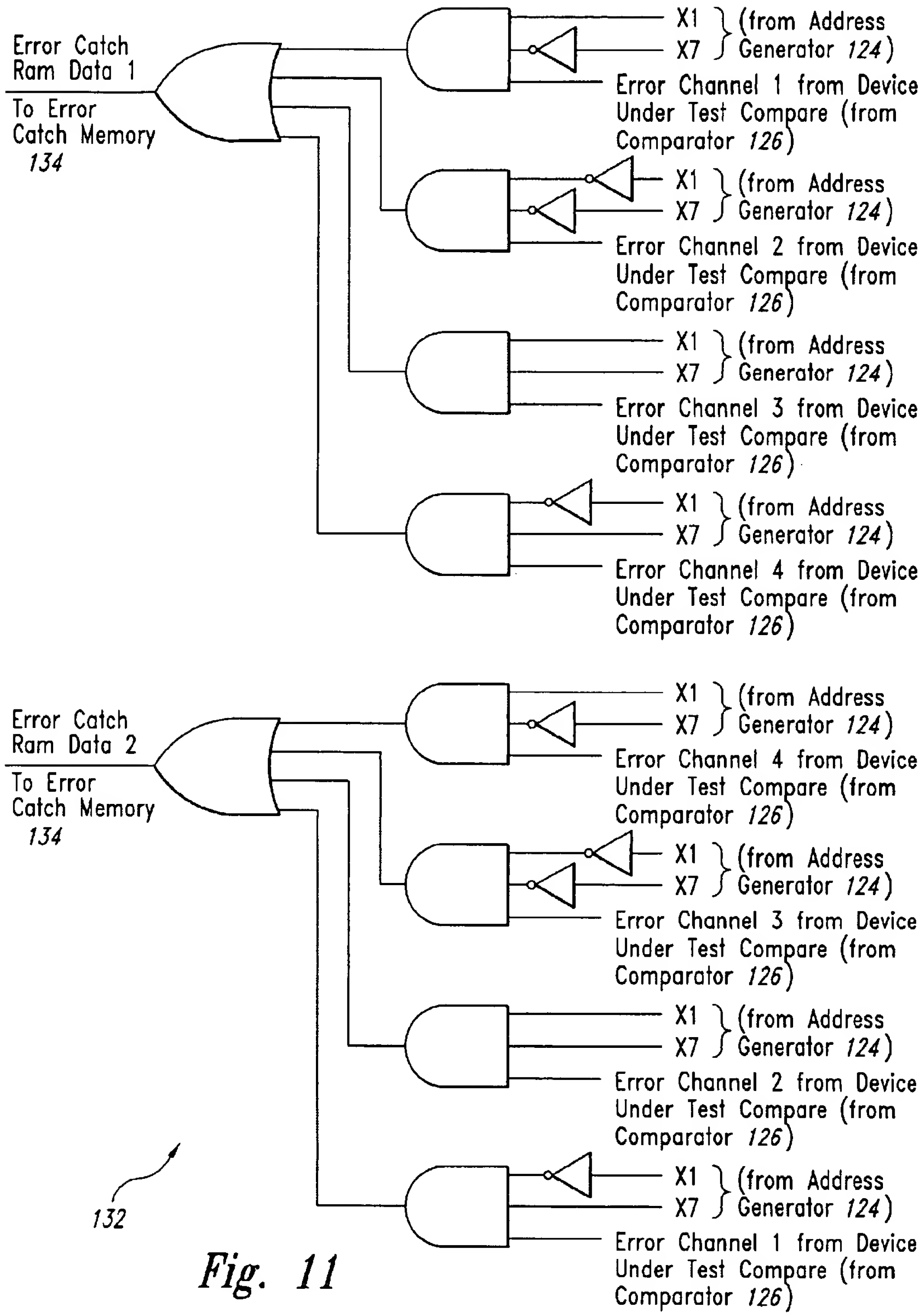

Error Catch
Ram Data 1
To Error
Catch Memory
134
X1
X7
(from Address
Generator 124)
Error Channel 1 from Device
Under Test Compare (from
Comparator 126)
X1
X7
(from Address
Generator 124)
Error Channel 2 from Device
Under Test Compare (from
Comparator 126)
X1
X7
(from Address
Generator 124)
Error Channel 3 from Device
Under Test Compare (from
Comparator 126)
X1
X7
(from Address
Generator 124)
Error Channel 4 from Device
Under Test Compare (from
Comparator 126)
Error Catch
Ram Data 2
To Error
Catch Memory
134
X1
X7
(from Address
Generator 124)
Error Channel 4 from Device
Under Test Compare (from
Comparator 126)
X1
X7
(from Address
Generator 124)
Error Channel 3 from Device
Under Test Compare (from
Comparator 126)
X1
X7
(from Address
Generator 124)
Error Channel 2 from Device
Under Test Compare (from
Comparator 126)
X1
X7
(from Address
Generator 124)
Error Channel 1 from Device
Under Test Compare (from
Comparator 126)
132

Fig. 11

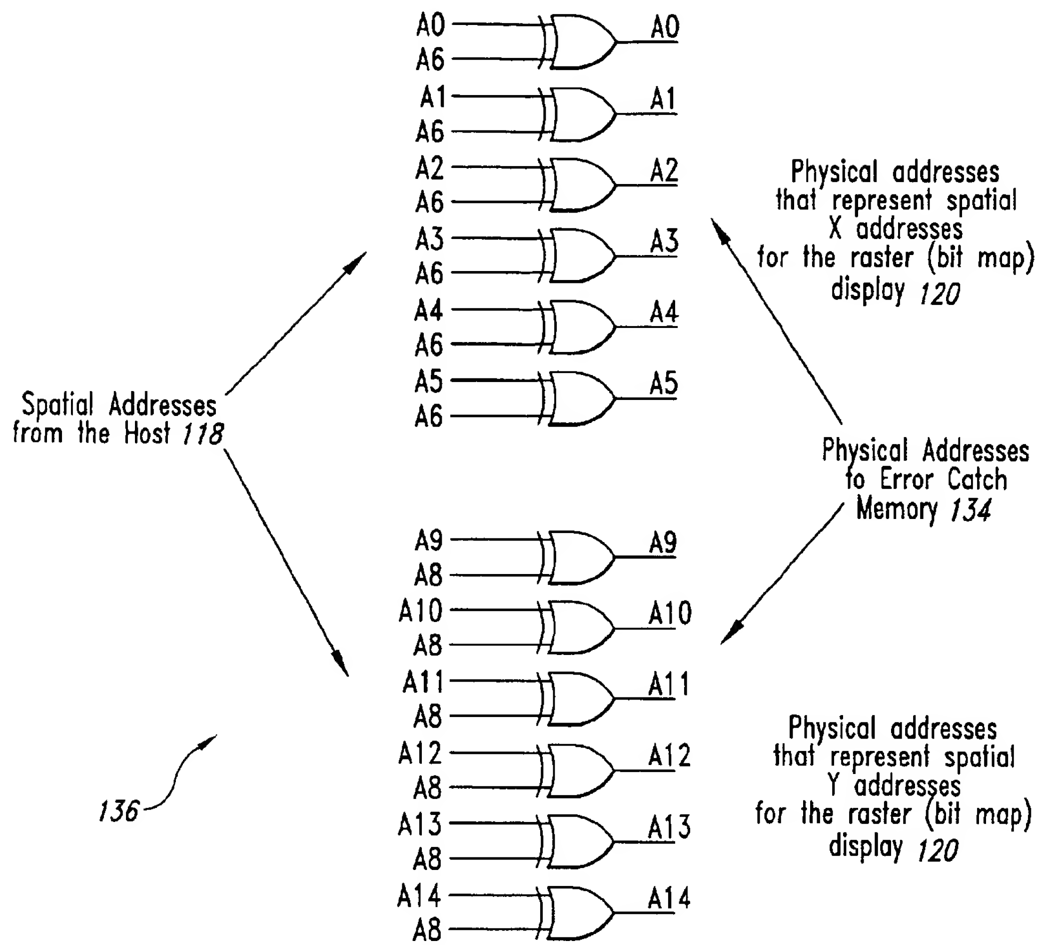

A0
A6
A0
A1
A6
A1
A2
A6
A2
A3
A6
A3
A4
A6
A4
A5
A6
A5
Physical addresses that represent spatial X addresses for the raster (bit map) display 120
Spatial Addresses from the Host 118
Physical Addresses to Error Catch Memory 134
A9
A8
A9
A10
A8
A10
A11
A8
A11
A12
A8
A12
A13
A8
A13
A14
A8
A14
Physical addresses that represent spatial Y addresses for the raster (bit map) display 120
136

Fig. 12

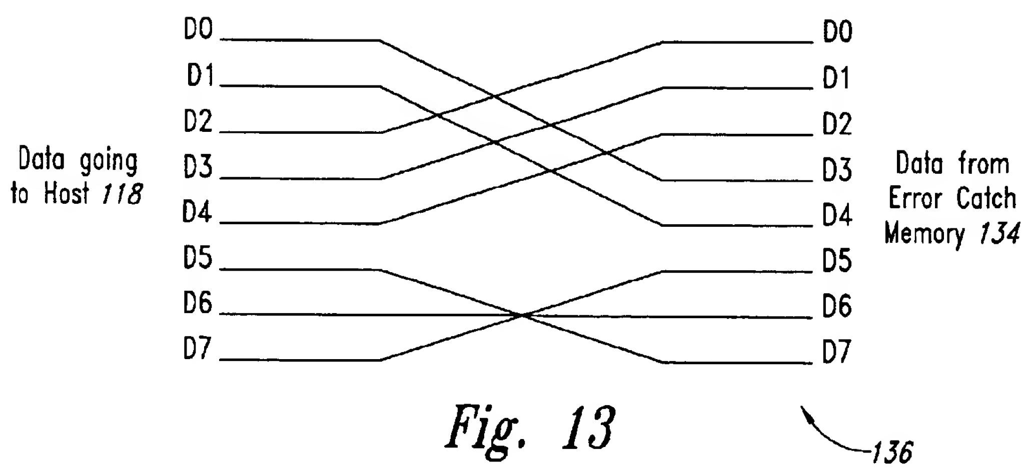

D0
D1
D2
D3
D4
D5
D6
D7
Data going to Host 118
D0
D1
D2
D3
D4
D5
D6
D7
Data from Error Catch Memory 134
136

Fig. 13

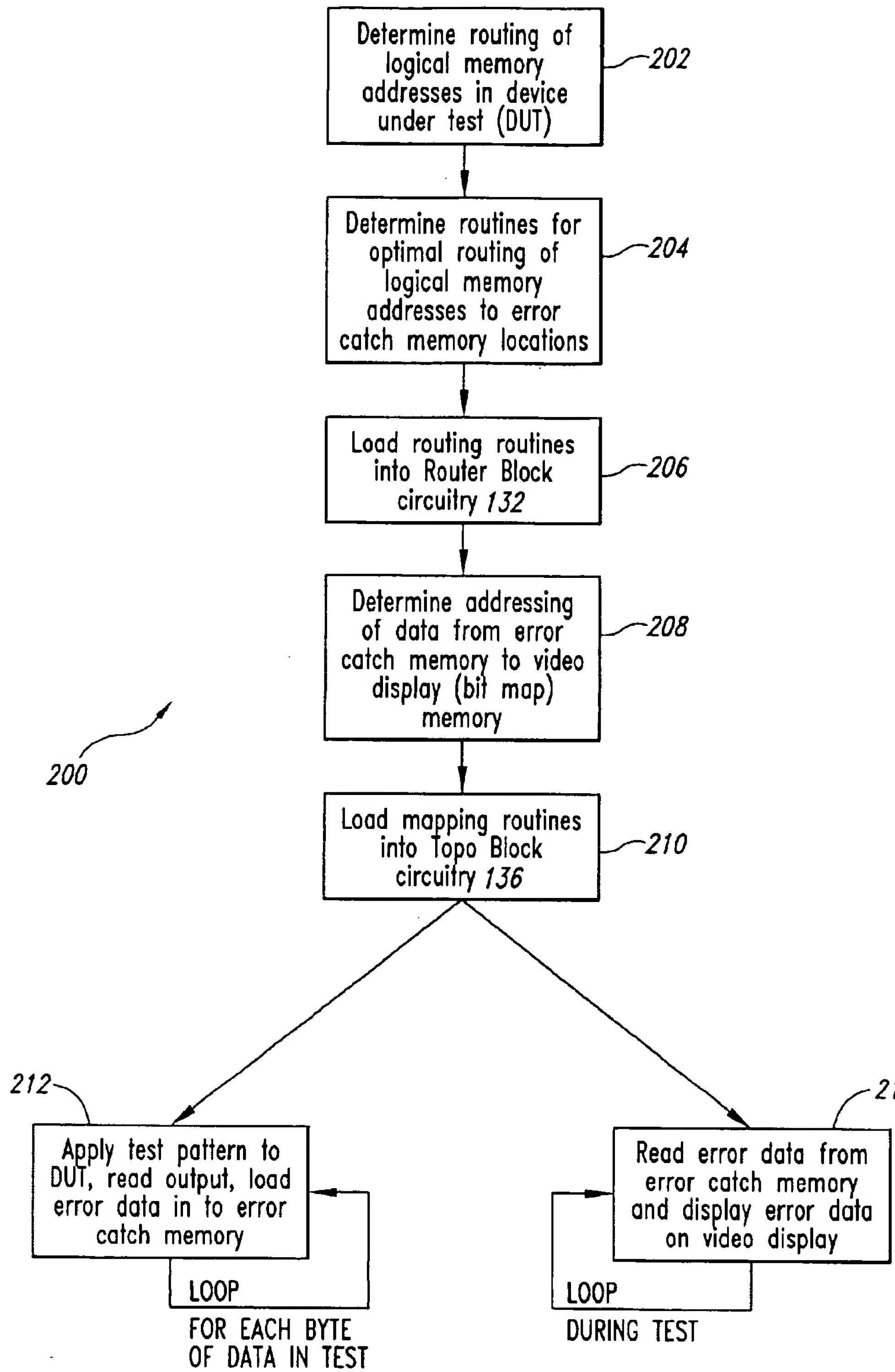

Determine routing of logical memory addresses in device under test (DUT)
202
Determine routines for optimal routing of logical memory addresses to error catch memory locations
204
Load routing routines into Router Block circuitry 132
206
Determine addressing of data from error catch memory to video display (bit map) memory
208
200
Load mapping routines into Topo Block circuitry 136
210
212
Apply test pattern to DUT, read output, load error data in to error catch memory
LOOP
FOR EACH BYTE OF DATA IN TEST
214
Read error data from error catch memory and display error data on video display
LOOP
DURING TEST

Fig. 14

METHOD AND APPARATUS FOR TESTING MEMORY DEVICES AND DISPLAYING RESULTS OF SUCH TESTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application No. 08/915,074, filed Aug. 20, 1997 now U.S. Pat. No. 6,134,677 which is a continuation of 08/567,069, filed Dec. 4, 1995, now U.S. Pat. No. 5,720,031.

TECHNICAL FIELD

The present invention relates to apparatus and methods for testing electrical devices, particularly semiconductor memory devices.

BACKGROUND OF THE INVENTION

Various types of errors can occur during the manufacture of semiconductor devices. As circuit density on semiconductor devices increases, the number of these errors can increase. For quality control and to improve yields of commercially acceptable semiconductor devices, the semiconductor devices are tested, often before a die containing the device is packaged. A series of probes on a test station contact pads on the die to thereby access portions of the semiconductor device.

For example, in a semiconductor memory device, the probes contact address pads to access selected memory cells in the memory device. A predetermined set or pattern of data is typically written to selected addresses that correspond to certain memory cells, and then the data is read from those memory cells to determine if the read data matches the data written to that address. If the read data does not match the written data, then the memory cells at the selected addresses are likely faulty.

A person testing several dies on the wafer can then examine a particular die itself, by means of a microscope, to determine the reason for such errors, e.g., whether the errors occurred from masking defects, during deposition of certain layers, and so forth. During the initial development of a semiconductor device, many different changes can be made to compensate for detected errors, including making changes to certain masks. Once a semiconductor device is in production, however, redundant circuitry on the semiconductor device can be employed to compensate for only certain detected errors.

One known apparatus for testing semiconductor wafers, manufactured by Teradyne Corporation, employs a test bed that receives the wafer, probes that contact the pads on each die in the wafer, and testing circuitry for applying addresses and writing data to, and reading data from, the dies by means of the probes. An error catch memory stores comparison signals from an error compare circuit that reflect errors located in the semiconductor wafer ("error data"). The error catch memory also receives addresses from an address generator circuit of locations on the die at which the errors occurred, such as the row and column or "logical addresses" of memory locations in a memory cell. A host computer retrieves the error data and the logical addresses from the error catch memory and displays the error data on a visual display such as a raster display CRT.

The host computer in the Teradyne apparatus maps the error data to spatial locations on the display device that correspond to physical locations on the die. As a result, the visual display shows an enlarged view of the die containing the semiconductor device and the locations on the semiconductor device that produced the error data (e.g., the locations of faulty memory cells). The person testing the semiconductor device can then see the locations of the errors on the device from the visual display and therefrom know where to inspect on the die to examine certain memory cells that produced the errors. The person can thereby possibly uncover manufacturing defects in the die.

Often, semiconductor devices employ logical addressing schemes that do not correspond to X and Y axis spatial locations on a visual display device. In a bitmapped display, the top leftmost pixel typically has a minimum coordinate value such as (0,0), while the lower right-hand pixel has a maximum coordinate value such as (528, 727). In a typical memory deice, employing only a single array of memory cells, a lower right comer of the array instead could have a minimum logical row and column address of (0,0) for the first bit in the device, while the upper right could have a maximum logical address that corresponds to the size of the array. A simple mapping algorithm is necessary to map the memory array locations to bitmap coordinates on the visual display.

Many complex memory devices produced today employ **16** or more arrays of memory cells on a single semiconductor device. Each array in the semiconductor device could itself have a logical addressing scheme that differs from those of neighboring arrays on the device. As a result, the host computer in the Teradyne apparatus must perform even more complex algorithms to map the logical addresses at which the errors occurred on the semiconductor device to spatial locations or "spatial addresses" on the visual display, which correspond to physical locations on the die at which the errors occurred. In other words, the host computer in the Teradyne apparatus must convert the logical addresses of a semiconductor device being tested to physical addresses, which correspond to physical locations on the device, and then convert the physical addresses to spatial addresses for bitmap display on the display device.

The complex algorithm employed by the host computer is inherently slow, particularly when many mapping algorithms must be performed for many addresses in a complex semiconductor memory device. If a person conducting the test desires to change addresses on the semiconductor device or input different parameters (e.g., higher voltage values), these addresses/parameters must be input to the testing circuitry, the testing circuitry initiated, and then the host computer must again perform the mapping algorithms to display new error data on the visual display. This process is inherently time consuming as a result of the logical-to-physical and physical-to-spatial mapping algorithms required to properly display error data on the display device. With a large number of dies to test on a single semiconductor wafer, and many memory locations on a given die itself to test, the time consuming process required by the Teradyne testing apparatus requires many man hours.

The time consumptive nature of this prior art method is exacerbated by the need to reload a different routine or employ a different testing circuit for different semiconductor devices, some of which may be on a single wafer. Therefore, if a memory device employing four memory cell arrays is initially tested, and then a memory device employing 16 memory cell arrays is later tested, a different algorithm must be loaded into the host computer and the testing circuitry must be modified for the new memory device before the 16 array device can be tested.

SUMMARY OF THE INVENTION

The present invention provides an apparatus and method for testing a semiconductor device, and in real-time, dis-

playing the spatial locations of errors on a display device, where the locations of the errors on the display device correspond to physical locations on a die containing the semiconductor device. The present invention preferably employs a field programmable gate array ("FPGA") or hardware implemented look-up table for rapidly routing the error data received from an error compare circuit to an error catch memory in a manner such that the error data is stored in the error catch memory at physical addresses that correspond to logical addresses employed by the device being tested. As a result, the router circuit continually routes error data to particular physical locations in the error catch memory. A topological circuit, such as an FPGA, remaps the physical locations of the error data from the error catch memory to spatial locations for display on a bitmapped display device such as a CRT. Therefore, the topological circuit can also continually route the error data from the error catch memory, through the host computer, for display on the display device. Overall, the router circuitry continually routes the logical addresses of error data to appropriate physical addresses in the error catch memory for the device being tested, while the topological circuitry continually maps the physical addresses of the error data to spatial addresses for display on the bitmap display device, all while the host computer is performing other functions such as applying a test pattern to the device, controlling the display device, etc.

By being implemented in hardware, the router and topological circuits are considerably faster than the prior alt approach of performing routines by the host computer. Additionally, the router and topological circuits can operate in parallel with the host computer, thereby improving the overall speed of the testing apparatus of the present invention. As a result, while the Teradyne system requires a mainframe or supercomputer for fast testing of complex semiconductor devices, the present invention can employ a minicomputer or personal computer as its host computer, thereby realizing a much more cost-effective testing apparatus. Moreover, since the router and topological circuits are programmable, the host computer can, at any time, reprogram them for different semiconductor devices to be tested, even during the testing of a given device. As a result, the testing apparatus of the present invention is exceptionally fast, flexible and able to provide true physical mapping of the device being tested.

In a broad sense, the present invention embodies an apparatus for assisting in the display of locations of errors in a semiconductor device on a display device for use in a testing system, the testing system having a computer and a visual display device. The semiconductor device has a plurality of memory locations, each addressable by logical addresses.

An error catch memory has a plurality of memory cells for storing error data, the en-or data corresponding to a comparison between data written to the plurality of memory locations in the semiconductor device, and data read from the plurality of memory locations. Each memory cell of the error catch memory is addressable by a physical address.

A programmable router circuit is coupled to the error catch memory and the semiconductor device. The programmable router circuit converts the logical addresses to physical addresses. The programmable router circuit thereby routes for storage the error data from the plurality of memory locations in the semiconductor device to selected memory cells in the error catch memory.

A programmable topological circuit is coupled to the error catch memory and the computer. The programmable topological circuit receives spatial addresses from the computer, and converts selected spatial addresses to selected physical addresses. The programmable topological circuit provides error data corresponding to the selected physical addresses to the computer in response to the spatial addresses. The programmable topological circuit thereby allows the error data from the semiconductor device to map to spatial addresses on the display device for displaying the locations of errors in the semiconductor device.

The present invention also embodies a method of testing a semiconductor memory device and displaying on a display device spatial locations of errors in the semiconductor device. The semiconductor device has a plurality of memory locations each addressable by logical row and column address signals. The method includes the steps of: (i) loading a routing routine into a routing circuit for converting the logical addresses of the semiconductor device to physical addresses, the routing routine being based on a layout of the memory locations in the semiconductor memory device; (ii) loading a mapping routine into a topological circuit for converting spatial addresses to physical addresses, the mapping routine being based on a layout of a plurality of memory cells in an error catch memory; (iii) continually applying a test pattern to the semiconductor device, determining error data from the semiconductor device and routing the error data to the error catch memory based on the routing routine; and (iv) substantially simultaneous with the step of continually applying a test pattern, constantly reading the error data from the error catch memory and displaying the error data at spatial locations on the display device based on the mapping routine.

The present invention furthermore embodies an apparatus for assisting in the display of locations of errors in a semiconductor device on the display device, the semiconductor device having a plurality of circuit locations addressable by logical addresses. The apparatus includes an error catch memory having a plurality of memory cells for storing the error data derived from the semiconductor device. A programmable router circuit is coupled to the error catch memory and the semiconductor device. The programmable router circuit converts the logical addresses to physical addresses to thereby route for storage the error data from the plurality of circuit locations in the semiconductor device to select the memory cells in the error catch memory. The error catch memory also provides error data corresponding to selected physical addresses to the computer in response to spatial addresses from the computer to thereby allow the error data from the semiconductor device to map to spatial addresses on the display device for displaying the locations of errors in the semiconductor device.

The present invention allows testing to be performed quickly and automatically over a wide array of semiconductor devices. Error mapping circuitry is electrically programmably reconfigurable so as to be modified to rapidly route error data from any number of semiconductor devices that may be tested to video memory for display on a display device. Other features and advantages under the present invention will become apparent from studying the following detailed description of the presently preferred embodiment, together with the following drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an isometric view of a testing apparatus of the present invention.

FIG. 2 is a block diagram of an error mapping circuit of the testing apparatus of FIG. 1 having an error catch memory, routing circuitry and topological circuitry.

FIG. 3 is an enlarged block diagram of the router circuitry of FIG. 2.

FIG. 4 is an enlarged block diagram of the topological circuitry of FIG. 2.

FIG. 5 is a block diagram of a one megabit by four semiconductor memory device, which shows logical and physical addresses for memory cells in the device, the device being capable of being tested by the testing apparatus of FIG. 1.

FIG. 6 is a front view of a visual display device of the testing apparatus of FIG. 1.

FIG. 7 is a schematic diagram of a logical gate array programmed into the router circuitry of FIG. 3 by the host computer based on the memory device of FIG. 5.

FIG. 8 is a schematic diagram of a logical gate array programmed into the topological circuitry of FIG. 4 by the host computer.

FIG. 9 shows how data lines are routed by the topological circuit of FIG. 4 from the error catch memory to the host computer.

FIG. 10 is a block diagram of the error catch memory of FIG. 2, which shows the physical and spatial addresses for the memory cells in the memory which are addressed by a host computer of the testing apparatus of FIG. 1, through the topological circuitry of FIG. 4.

FIG. 11 is a schematic diagram showing an example of another logical gate array that can be programmed into the router circuitry of FIG. 3 by the host computer.

FIG. 12 is a schematic diagram of an example of another logical gate array that can be programmed into the topological circuitry of FIG. 4 by the host computer.

FIG. 13 shows an example of how data lines can be redirected by the topological circuit of FIG. 4 from the error catch memory to the host computer.

FIG. 14 is a flow chart showing the preferred steps performed by the testing apparatus of FIG. 1.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS OF THE INVENTION

Referring to FIG. 1, a testing apparatus **100** of the present invention includes essentially two stations, a testing station **102** and an analysis station **104**. A test bed **106** in the testing station **102** releasable secures a wafer **108**, which has one or more dies or semiconductor devices, including a device **107** formed thereon. The test bed **106** can have a motor-controlled securing device for moving the wafer under control of the analysis station **104**. A microscope **110** positioned over an upper surface of the wafer **108** allows a user to visually inspect desired portions of the devices **107** on the wafer.

A series of test probes **112** electrically couple to pads on the device **107** to provide means for writing addresses and data to, and reading data from, semiconductor circuits on the device **107** in the wafer **108**. One or more cables electrically and/or optically couple the probes **112** and the test station **102** to the analysis station **104**.

A device under test interface **116**, which forms part of the analysis station **104**, provides appropriate routing, scaling, amplification or other signal processing for signals written to, or read from, the device **107**. A host computer **118**, having a visual display device **120** such as a CRT, and a keyboard **122**, performs most operations in the analysis station **104**. The host computer **118** produces test data or a test pattern which is applied to the device **107** on the wafer **108** being tested (i.e., the device under test or "DUT"). An address generator **124** provides addresses for writing data to, and reading data from, the device **107**. An error counter and comparator **126** compares the data written to the device **107** to the data read from the device to determine if an error has occurred, and increments a counter for each such error.

A timing and control circuit **128** provides the appropriate signals for reading to and writing from the device **107**. A display capture and adjustment circuit **129**, having several programmable control knobs, provides means for adjusting analysis and display parameters such as zooming into, and out of, display of the device **107** as the device is displayed on the display device **120**. Error mapping circuitry **130** provides the mapping of logical-to-physical addresses, and physical-to-spatial addresses, as described in more detail below. The analysis station **104** is generally shown as a series of rack-mounted components to represent the electrical interconnection between the host computer **118** with the device under test interface **116**, address generator **124**, error comparator circuitry **126**, timing and control circuitry **128**, display capture and adjustment circuitry **129** and error mapping circuitry **130**. The host computer **118** is preferably a microcomputer or personal computer, while the device under test interface **116**, address generator **124**, error comparator **126**, timing and control circuitry **128** and display capture and adjustment circuitry **129** are generally known by those skilled in the semiconductor testing art.

Referring to FIG. 2, the error mapping circuitry **130** includes a router block or circuitry **132** that receives row and column logical addresses from the address generator **124**, and receives the error data regarding the device **107** from the error comparator **126**. As explained in more detail below, the router circuitry **132** maps the logical addresses of the device **107** to physical addresses for storing the error data in an error catch memory **134**. The error catch memory **134**, preferably high-speed random access memory ("RAM"), stores the error data produced from the device **107** in physical locations that correspond closely to the physical locations of memory cells, or arrays of memory cells, in the device. (The terms "location" and "address" are often used interchangeably herein.) Therefore, as shown in FIG. 2, the error catch memory **134** contains a large two-dimensional array of blocks **135** of memory cells. FIG. 2 shows an exemplary 6×6 array of memory cell blocks **135**, a total of **36** blocks, for the error catch memory **134**.

Each block **135** of memory in the error catch memory **134** preferably has a separate input error channel for data. To be flexible and thereby be adaptable to various types of semiconductor devices to be tested, the error catch memory **134** can have a substantially larger number of memory blocks **135**, each block having a relatively small number of memory cells. As a result, the router circuitry **132** can be configured so that routing of error data causes several blocks **135** of the error catch memory **134** to be grouped together for storing the error data from a larger memory array in the device **107**. For simplicity, however, and as described more fully below, sixteen of the blocks of memory in the error catch memory **134** are shown as having error channels ED1-ED16 for storing error data from sixteen blocks of memory in the device **107**.

A topological block or circuitry **136** receives spatial addresses from the host computer **118** for addressing error data in the error catch memory **134** for display on the display device **120**. The topological circuitry **136** maps the spatial addresses received from the host computer **118** to the appropriate physical address in the error catch memory **134**,

and thereby accesses the appropriate error data from the memory. After mapping the spatial address from the host computer **118** to physical addresses in the error catch memory **134**, the topological circuitry **136** then retrieves the appropriate error data to be displayed or stored in video memory (not shown) in the host computer **118** which drives the display device **120**. As a result, the topological circuitry **136** properly maps the error data in the error catch memory **134** to the video memory in the host computer **118** so that the physical addresses or locations of the error data in the error catch memory **134** are stored in the video memory for proper display at spatial locations on the display device **120**.

For example, the top left-most pixel of the display device **120** can have a spatial address of (0,0), which corresponds to row and column address (0,0) in the video memory. To display this pixel on the display device **120**, the host computer **118** requests data at address (0,0) from the error catch memory **134** for storage at row and column address (0,0) in the video memory. The topological circuitry **136** receives the spatial address request from the host computer **118** and, based on the orientation of the device **107** in the test bed **106**, retrieves the appropriate error data bit from the error catch memory **134** so that error data for the upper left-most memory cell in the device is displayed at this pixel. Due to the differences in addressing between the physical addresses of the error catch memory **134**, and the spatial addresses of the display **120** (or video memory), the topological circuitry **136** must translate or map the spatial addresses received from the host computer **118** into appropriate physical addresses so that the appropriate error data is retrieved from the error catch memory **134** for appropriate display on the display device **120**.

Importantly, the host computer **118** continually and sequentially applies the preselected test pattern to the device **107**, typically from an initial row and column address of (0,0) through increasing addresses (in row and/or column fashion). Similarly, the host computer **118** continually addresses the error data stored in the error catch memory **134** for its display on the display device **120** in a similarly incrementing sequential addressing method. As a result, the router circuitry **132** continually routes the error data received from the error comparator **126** to appropriate locations in the error catch memory **134**, as the incoming addresses are sequentially incremented. Similarly, the topological circuitry **136** continually maps the error data from the error catch memory **134** to video memory in the host computer **118** in response to sequential addresses received by the host computer, so that the stored error data is appropriately displayed on the display device **120**.

As explained more fully below, the router and topological circuits **132** and **136** must be programmed to perform the particular routing and mapping of logical addresses to physical addresses, and physical addresses to spatial addresses, for each semiconductor device to be tested. As a result, the router and topological circuits **132** and the router circuitry **136** are preferably field programmable logic or gate arrays ("FPGAs"), as shown in FIGS. **3** and **4**, respectively.

FPGAs typically have an array of logic modules interspersed with a programmable interconnect architecture. Under the present invention, the logic modules themselves are preferably programmable. Input/output pads for the FPGA may be programmable to be an input, an output, or a bidirectional I/O circuit for use in a bus which connects with the host computer **118** and the error catch memory **134**. FPGAs allow logic designs of relatively low complexity to be readily implemented and reprogrammed using known software provided with such arrays. As a result, FPGAs allow a variety of logic circuits to be implemented using a single device. Different programming technologies, such as anti-fuses, non-volatile memory elements, memory element controlled switches, etc., can be used in FPGAs. Overall, FPGAs are known by those skilled in the art, and the present invention preferably employs static random access memory ("SRAM") implemented FPGAs so that they can be readily programmed by the host computer **118**.

The host computer **118** performs a programming setup for the router circuitry **132** and topological circuitry **136** for each type of semiconductor device tested, since each type of device likely has its own particular physical layout that differs from a sequentially incremented logical address scheme employed by the host. The host computer **118** therefore programs the router circuitry **132** as a predetermined set of logic gates, as described below, to accommodate the layout of the device **107**. Additionally, the host computer **118** programs the topological circuitry **136** as a predetermined set of logic gates to accommodate the differences in layout between the coordinates of the bit map display of the display device **120**, and its corresponding video memory in the host computer **118**, and the layout of the error catch memory **134**.

Referring to FIG. **5**, an exemplary block diagram of a one meg by four semiconductor memory device is shown having four memory cell arrays DQ1–DQ4 that are each subdivided into four blocks, represented by subscripts through "4". By dividing the memory into four memory cell arrays DQ1–DQ4, data is multiplexed so that each memory array is addressed by its own data line, and therefore the device **107** has four data lines DQ1–DQ4. As is known in the art, during a write cycle, the host computer **118** causes a four bit byte of test data to be driven onto the data lines DQ1–DQ4 for storage in each of the corresponding memory arrays DQ1–DQ4, based on a logical address the host simultaneously applies to the device. The device **107** stores one bit of the test data byte in a particularly addressed memory location in each of the four memory arrays DQ1–DQ4. Since the device **107** is a one megabit by four memory device, 1,024 row lines and 1,024 column lines are used to access one of over 1 million memory cells in each of the four memory cell arrays DQ1–DQ4.

As shown along the top and left side of the device **107** in FIG. **5**, the logical addresses for accessing the various blocks of memory cells differs from the physical addresses of such memory cells. For example, if the device **170** were simply a four megabit by one memory device, the logical addresses could be equivalent to the physical addresses, so that the first memory location in the upper left corner of the block $DQ1_1$ of memory locations would have a logical and physical address of (0,0) which corresponds to the row and column address, and x and y axis physical locations, of the memory cell, all respectively. Similarly, in this example, the most lower right hand memory location in the block $DQ2_4$ would have the logical and physical address of (2047,2047).

For reasons of fabrication ease, to reduce line capacitances, and to improve the overall performance of the device **107**, the blocks of memory cells, for the four arrays of memory cells DQ1–DQ4, are arranged in predetermined patterns. For example, a single memory location **140** in the memory block $DQ4_2$ has a logical row and column address of (384,640), but has a physical address or location of (1152,896). As shown, the logical row addresses for bits **0–511** ascend from left to right for the block $DQ1_1$, but its adjacent block $DQ3_1$ has row addresses that descend from left to right from **511** to **0**. A vertical dashed line shown in FIG. **5** helps visually show that the memory blocks are

mirrored in the device **107**. In other words, the blocks $DQ1_1$, $DQ2_1$, $DQ1_3$ and $DQ2_3$ are accessed by logical row addresses **0–511** in left to right order, while the memory cell blocks $DQ3_1$, $DQ4_1$, $DQ3_3$, and $DQ4_3$ are accessed by logical row addresses **511–0** from left to right. The other columns of memory blocks are similarly mirrored in the device **107**. Other semiconductor devices known by those skilled in the relevant art have similar mirrored layouts, or other arrangements of memory blocks.

Referring now to FIG. **6**, an exemplary front view of the visual display **120** for displaying error data for the device **107** has a raster or bit map display portion **144**. The bitmap display portion **144** includes a visual representation of the memory device **107** as a large square, with the exemplary memory location **140** noted above being shown as a dot **140'**, if the memory location were flagged as an error. The display **120** also has various positions that provide the user with a display of relevant information during the testing of the device **107**. A portion **146** of the display **120** shows the cursor position. A portion **148** of the display **120** shows a size of the zoom for the bit map display portion **144** (in bits/pixel), and a portion **149** shows a zoom tracker display which shows the location of the zoom, thereby allowing a user to zoom into a particular portion of the device **107**.

A portion **150** shows a total number of errors for each memory cell array DQ1–DQ4, while a portion **152** displays the status of the errors currently being displayed. A portion **154** shows the values of various input and output voltages for the power supply to the device **107**. A portion **156** shows the size, in logical addresses, of the area displayed in the bitmap display portion **144**. A portion **158** shows a refresh rate of the display **120**.

A portion **160** shows a representation of the four knobs of the display capture circuitry **129** (FIG. **1**) with a value of a corresponding parameter assigned to the knob. Importantly, the knobs can be programmed by the analysis station 104 to allow a user to adjust the parameters of input signals applied to the device **107**, and under the present invention, view in real time the results of such changes. For example, the user can adjust the power supply voltage Vcc to see how changes in the voltage affect the device **107**. Finally, a portion **162** shows a quick reference of the functions assigned to function keys F1–F12 of the keyboard **122**, while portion **164** shows the particular test pattern being applied by the host computer **118** to the device **107**.

As explained above, the router and topological circuits **132** and **136** are programmed by the host computer **118** to emulate predetermined networks of logic gates to provide routing of logical to physical addresses and mapping of physical to spatial addresses. FIG. **7** shows an example of a set of logic gates programmed by the host computer **118** and emulated in router circuitry **132**. As shown in FIG. **7**, the router circuitry **132** is programmed to emulate sixteen 3-input AND gates, some of which have inverting inputs. Each of the AND gates provides an error channel output to one of sixteen blocks **135** of memory ECD1–ECD 16 in the error catch memory **134** (FIG. **2**). Two of the three inputs to the AND gates are selected bits of addresses received from the address generator **124**, while the third input is error data received from one of the four memory arrays DQ1-DQ4 from the device **107** (received through the error comparator **126**). The two address inputs are either inverted or not inverted so that the AND gates receive different combination of the two address inputs.

The two address inputs are the tenth bits of 11-bit row and column address (shown as "X9" and "Y9" for the row and column logical addresses, respectively). Therefore, when the decimal logical row address changes from 511 to 512, the tenth significant bit **X9** in the binary logical row address changes from 0 to 1 (i.e., from "00111111111" to "01000000000."). As a result, the logic gates emulated by the router circuitry **132** switch from outputting error data over error channels ECD1, ECD2, ECD5, ECD6, ECD9, ECD10, ECD13 and ECD14 to outputting error data over error channels ECD3, ECD4, ECD7, ECD8, ECD11, ECD12, ECD15 and ECD 16 to the respective block **135** in the error catch memory **134** (see FIG. **2**). (The remaining blocks of memory in the error catch memory **132**, and therefore other error channels to such memory, are ignored by the router circuitry **132**.) By using programmed logic gates, rather than software routines, the router circuitry **132** can rapidly route error data from the blocks of memory in the four memory arrays of the device **107** to corresponding blocks of memory in the error catch memory **134**. (For ease of understanding, the router circuitry **132** is described at times herein as retrieving error data from the device **107**; in actuality, as described above, the error data is received from the error comparator **126**.)

Importantly, the router circuitry **132** attempts to route the error data from the locations of the data in the device **107** to corresponding locations in the error catch memory **134** so that the layout of the error data in the error catch memory is physically arranged in a manner similar to its layout in the device, despite differences in addressing employed between the error catch memory and the device. As a result, the error catch memory attempts to emulate the exact layout of the device.

The above-described example assumes, for simplicity, that each block **135** in the error catch memory **134** has a sufficient size to store each block of memory DQ1–DQ4 from the device **107**. As noted above, the error catch memory **134** preferably includes multiple smaller blocks of memory that can be combined to accommodate various size blocks of memory in a given device being tested.

Referring to FIG. **8**, the topological circuitry **136** is similarly programmed by the host computer **118** to emulate arrays of logic gates necessary for routing physical addresses in the error catch memory **134** to spatial addresses for displaying error data on the display **120**. FIG. **8** shows a series of nine 2-input exclusive OR gates that each receive the address **A9** and one of the addresses **A0–A8**. A tenth exclusive OR gate receives the address **A10** and the output of an AND gate that receives at its inputs the addresses **A9** and **A10**. The remaining addresses **A9** and **A11–A21** are routed directly through the topological circuitry **136** from the error catch memory **134** to the host computer **118**.

As a result, the ten exclusive OR gates produce address values **A0–A8** and **A10**, that with the address values **A9** and **A11–A21**, are input to the error catch memory **134** for addressing memory therefrom in a serial manner consistent with addresses received from the host computer **118** (typically based on the layout of the video memory). In other words, the logic gates of FIG. **8** implemented by the topological circuitry **136** address the appropriate portions of the error catch memory **134** for direct bitmap display of the error data on the display device **120** in response to serially incremented addresses received by the host computer **118**.

The particular configuration of exclusive OR gates of FIG. **8** programmed by the host computer **118** into the topological circuitry **136** compensates for or maps the mirroring layout of row addresses for blocks in the device **107**. As explained above, the row addresses 0–511 for DQ1

are mirrored for DQ3 about the dashed line in FIG. 5. By simply exclusive ORing the tenth significant address bit (A9) with each of the less significant address bits (A0–A8), the topological circuitry 136 can access the error data in the error catch memory 134 in a serial manner with a string of incremented addresses input by the host computer 118 for display of data on the display device 120. Since the column addresses are not mirrored, direct routing of address lines A11–A21 are performed by the topological circuitry 136.

The example of FIG. 8 assumes that the video memory employed for spatially addressing bitmap locations on the display device 120 is performed in a direct, serially incremented manner of addresses for an initial binary row and column addresses of 000000000 (for addresses A0–A10 and A11–A21, respectively) to the maximum spatial address for the display device 120. Therefore, as shown in FIG. 9, the error data from the error catch memory 134 can be remapped to portions of the video memory in the host computer 118. For the above-described example, error data from each block EDC1–EDC16 is directly routed to blocks of video data VD1–VD16. As shown along the top and left side of the error catch memory 134 in FIG. 10, the topological circuitry 136 stores the error data in blocks of memory EDC1–EDC16 that each have physical row and column addresses of 0–511. The spatial addresses requested by the host computer 118 for displaying error data on the display 120, however, are shown as serially incrementing, in row and column fashion, from 0 to 2047. As explained above, the topological circuitry 136 maps the physical addresses to the spatial addresses. Of course, the topological circuitry 136 can be programmed in alternate ways by the host computer 118 to provide mapping appropriate for various displays 120 and video memory used in bitmapping the display.

As explained above, the router and topological circuitry 132 and 136 can be programmed by the host computer 118 to emulate various logic gate networks and thereby rapidly route and/or map error data to and from the error catch memory 134. FIG. 11 shows an example of another logic gate network that can be emulated by the router circuitry 132. The example of FIG. 11 shows two of four sets of logic gates, where each set includes four 3-input AND gates whose outputs are provided to a 4-input OR gate. Two of the three inputs to the AND gates are the second and eighth significant address bits (shown as "X1" and "X7" for row logical addresses), while a third input is error data from one of the four memory arrays DQ1–DQ4. The address inputs are either inverted or not inverted so that each AND gate receives a different combination of two address inputs. As a result, each of the four sets of logic gates provides error data from each of the four memory cell arrays DQ1–DQ4 in the device 107 to the error catch memory 134. The example of FIG. 11 is directed to a semiconductor memory device (not shown) having more complex layout than that shown in FIG. 5.

A FIG. 12 similarly shows another example of logic gates that can be emulated in the topological circuitry 136 by the host computer 118. The example of FIG. 12 is directed to a semiconductor memory device where the lower significant address bits are mirrored with the address bit A6, while the higher significant address bits are mirrored with respect to address bit A8.

FIG. 13 shows an example of how the topological circuitry 136 can reroute the data lines from the error catch memory 134 to the host computer 118. The example of FIG. 13 is particularly directed to intertwined DQ lines where the layout of arrays of data cells in the error catch memory 134 differs from the layout of memory cell arrays in the video memory of the host computer 118. The examples of FIGS. 10–13 are only provided by way of example to help those skilled in the art recognize the various alternative configuration of logic gates and data line rerouting that can be programmed into the router circuitry 132 and the topological circuitry 136 by the host computer 118, and such examples do not relate to the previously described examples of FIGS. 5–9.

The testing apparatus 100 of the present invention is preferably performed under direction of a routine stored in and running on the host computer 118. Referring to FIG. 14, a preferred routine 200 performed by the testing apparatus 100 begins in step 202 where the host computer 118 determines the routing pattern for the logical memory addresses in the device being tested, such as the device 107. The host computer 118 preferably includes a mass storage device (not shown) for storing routing information for various types of devices to be tested by the apparatus 100 (e.g., various types of memory devices). If the host computer 118, however, does not have a previously stored routing, then the user must analyze the layout of logical addresses for the device then being tested.

In step 204, the host computer 118 determines which of many routing routines stored in the mass storage are optimal for routing the logical memory addresses for the device 107 to the error catch memory 134. Again, the host computer 118 preferably has stored in mass storage a large number of routing routines, and their corresponding logical gate arrays for implementing these routines. If the host computer 118 does not have an appropriate optimal routing routine stored in its mass storage, then the user must compare the layout of logical addresses in the device 107 to the layout of the blocks of memory 135 in the error catch memory 134 to determine an optimal routing for the logical addresses to physical addresses in the error catch memory. Thereafter, the user must determine what configuration of logic gates will provide such a routing. In step 206, the host computer 118 loads the selected optimal routing routine into the routing circuitry 132 so as to implement the routing routine in an array of logic gates (such as the gates shown in FIG. 7).

In step 208, the host computer 118 determines the mapping of error data in the error catch memory 134 to spatial addresses or addresses in video display memory, and selects the appropriate routing routine. If no such routine is stored in mass storage, then the user must determine the appropriate routine and its configuration in logic gates. In step 210, the host computer 118 loads the mapping routine into the topological circuitry 136 (such as that shown in FIGS. 8 and 9).

In step 212, the host computer 118 applies a user selected test pattern to the device 107 (through the address generator 124, timing and control circuit 128 and device under test interface 116). In step 212, the host computer 118 also causes the data to be read out from the device 107, compared to the written data (through the error comparator 126) and causes the error data to be loaded into the error catch memory 134 by means of the router circuitry 132. The step 212 continually loops during testing for each address and each bit, nibble, byte or set of data in the test pattern for the device 107.

Simultaneous with step 212, the host computer 118 in step 214 causes the error data to be read from the error catch memory 134, through the topological circuitry 136. The error data read from the error catch memory 134 is then displayed on the display 120 to thereby display, in real time, errors discovered or forced in the device 107. The step 214

is continually performed during the test to continually display errors, even as certain parameters of signals applied to the device **107** are changed.

The present invention is described above as implementing the router and topological circuitry **132** and **136** as FPGAs. In an alternative embodiment, the router and topological circuitry **132** and **136** can be implemented as lookup tables stored in certain programmable memories such as PROM, electrically erasable programmable read-only memory ("EEPROM"), flash memory, etc. Such lookup tables, rather than employing a routine implemented in logic gates, simply reroute or remap the logical addresses of the device **107** to corresponding physical addresses (for the router circuitry **132**), or physical addresses to spatial addresses (for the topological circuitry **136**). The lookup table in the router circuitry **132** essentially stores the translation of logical to physical addresses as shown along the top and left side of FIG. **5**, while the lookup table in the topological circuitry **136** essentially stores the translation of physical to spatial addresses shown along the top and left side of FIG. **10**.

For example, the lookup table in the router circuitry **132** can reflect that the memory location **140** (FIG. **5**) having a logical row and column address of (384,640) in the fourth memory array DQ4 has a physical row and column address of (1152,896). As a result, the lookup table can, in hardware, rapidly map the one megabit by four device **107** of FIG. **5** to a four megabit memory emulated in the error catch memory **134**. The alternative embodiment employing lookup tables, however, may require more processor time by the host computer **118**, and therefore may be slightly slower than the previously described embodiment employing FPGAs.

Overall, the present invention has been described above with respect to an exemplary embodiment for a one megabit by four device **107** being tested. The router and topological circuitry **132** and **136** can emulate logic gates having a greater or lesser number of addresses depending upon the size of the device **107** being tested, the size and layout of the error catch memory **134** and the video memory, and the number of bytes of error data that can be transferred at one time. Therefore, while sixteen error channels EDC1–EDC **16** are described above for the four memory cell arrays DQ1–DQ4, and sixteen error catch RAM data blocks respectively receive error data from such arrays, a greater or lesser number of channels from the device **107** being tested can be received by the router circuitry **132**, and the router circuitry can output a greater or lesser number of channels to the error catch memory **134**.

The present invention allows testing to be performed quickly and automatically over a wide array of semiconductor devices. The error mapping circuitry **130** is electrically or programmably reconfigurable so as to be modified to rapidly route error data from an indefinite number of semiconductor devices that may be tested to video memory for display on a display device. In a broad sense, if the physical addresses of the error catch memory **134** can map directly to the spatial locations on the display device **120** (and thus to the video memory), then the mapping circuitry **130** of the present invention can be implemented with only the router circuitry **132** and the error catch memory **134**.

While the detailed description has been expressed, in part, in terms of specific examples, those skilled in the art will appreciate that many other variations could be used to accomplish the purpose of the disclosed invention. For example, those skilled in the art will recognize that while the present invention described above for testing memory circuits, the invention can be readily adapted to test other semiconductor devices or circuitry. Accordingly, it can be appreciated that equivalent modifications to the above-described embodiments can be made without departing from the spirit and scope of the invention. Therefore, the present invention is limited only by the following claims.

What is claimed is:

1. A method for testing memory locations in a memory array of a memory device, comprising:

testing a first memory location in the memory array;

writing test results for the first memory location to a location in a test memory corresponding to a physical address;

mapping a spatial address of a display memory to the physical address;

reading the test results from the location corresponding to the physical address and storing the test results in a location in a display memory corresponding to the spatial address; and

testing a second memory location in the memory array.

2. The method of claim **1**, further comprising reading the test results from the display memory and displaying the test results at a location on a display corresponding to the spatial address.

3. The method of claim **1** wherein the first memory location corresponds to a first logical address and further comprises mapping the first logical address to a physical address in the test memory and writing the test results to the location in the a test memory corresponding to the physical address.

4. The method of claim **1** wherein mapping the spatial address to the physical address comprises referencing a look up table using the spatial address, the look up table storing the spatial address and having the physical address associated therewith.

5. The method of claim **1** wherein mapping the spatial address to the physical address comprises applying the spatial address to logic gates having outputs at which the physical address is provided.

6. A method for testing memory locations in a memory array of a memory device, comprising:

testing a memory location in the memory array corresponding to a logical address;

mapping the logical address of the memory location to a physical address;

storing test results for the tested memory location at a location in a test memory corresponding to the physical address; and

testing another memory location in the memory array.

7. The method of claim **6**, further comprising:

mapping a spatial address of a display memory to the physical address corresponding to the location in the test memory at which the test results are stored; and

reading the test results from the location in the test memory and storing the test results in a location in the display memory corresponding to the spatial address.

8. The method of claim **7**, further comprising reading the test results from the display memory and displaying the test results at a location on a display corresponding to the spatial address.

9. The method of claim **6**, further comprising:

mapping a spatial address of a display memory to the physical address corresponding to the location in the test memory at which the test results are stored;

reading the test results from the location in the test memory and storing the test results in a location in the display memory corresponding to the spatial address; and

reading the test results from the display memory and displaying the test results at a location on a display corresponding to the spatial address,

wherein the process of mapping the spatial address, reading from test memory, storing in the display memory, reading from the display memory and displaying the test results are sequentially performed for each spatial address before repeating for a next spatial address.

10. The method of claim 6 wherein mapping the logical address to the physical address comprises referencing a look up table using the logical address, the look up table storing the logical address and having the physical address associated therewith.

11. The method of claim 6 wherein mapping the logical address to the physical address comprises applying the logical address to logic gates having outputs at which the physical address is provided.

12. A method for testing memory locations in a memory array, comprising:

producing test results for a memory location corresponding to an address defined in a logical address space;

mapping the address of the tested memory location into a physical address space;

storing the test results for the tested memory location at a test memory location corresponding to the physical address space; and

producing test results for a next memory location.

13. The method of claim 12, further comprising:

mapping an address defined in a spatial address space to an address defined in the physical address space;

reading the test results stored at the corresponding address in the physical address space;

storing the test result in a location in a display memory corresponding to the address defined in the spatial address space.

14. The method of claim 13, further comprising reading the test results from the display memory and displaying the test results at a location on a display corresponding to the spatial address.

15. A method for testing a memory device having a plurality of memory locations addressable by logical address, the method comprising the steps of:

loading a routing routine, based on a layout of memory locations in the memory device, which converts logical addresses of the memory device to physical addresses of an error memory;

applying a test pattern to the memory device; and

substantially simultaneously with applying the test pattern, determining error data from the memory device and routing it to the error memory according to the routing routine.

16. The method of claim 15, further comprising:

loading a mapping routine based upon the layout of a plurality of memory cells within the error memory into a topological circuit for converting spatial address to physical addresses; and

substantially simultaneously with applying the test pattern, constantly reading the error data from the error memory and displaying the error data at spatial locations on a display device based upon the mapping routine.

17. The method of claim 15 wherein loading the routing routine comprises loading a routine into a field programmable gate array.

18. The method of claim 15 wherein loading the routing routine comprises loading a routine into a read only memory that stores a look-up table for converting the logical addresses to physical addresses.

19. A method of testing a semiconductor device and outputting locations of errors in the semiconductor device, the semiconductor device having a plurality of locations addressable by logical address signals, the method comprising the steps of:

programming a converter for converting spatial addresses to physical addresses based on a layout of a plurality of memory locations in an error memory;

applying test signals to the semiconductor device, determining error data from the semiconductor device and routing the error data to the error memory; and

reading the error data from the error memory and visually outputting the error data at spatial locations based on the programmed converter.

20. The method of claim 19, further comprising:

programming a router for converting the logical addresses of the semiconductor device to physical addresses based on a layout of the locations in the semiconductor device; and

routing the error data to the error memory based on the programmed router.

21. The method of claim 19 wherein programming the converter comprises loading a routine into a field programmable gate array.

22. The method of claim 19 wherein programming the converter comprises loading a routine into a read only memory that stores a look-up table for converting the spatial addresses to physical addresses.

23. A test circuit for identifying errors in a memory device having a plurality of memory locations addressable by logical addresses, the test circuit comprising:

an error memory addressable by physical addresses for storing error data corresponding to a comparison between data applied to the plurality of memory locations in the memory device and data read from the plurality of memory locations; and

a mapping circuit coupled to the error memory and the memory device, the mapping circuit mapping the logical addresses of the memory device to physical addresses in the error memory at which the error data from the plurality of memory locations in the memory device are to be stored.

24. The test circuit of claim 23, further comprising a display memory and an address translation circuit coupled to the error memory, the translation circuit adapted to receive spatial addresses corresponding to locations in a display memory and to translate the spatial addresses to physical addresses from which error data are read, the error memory providing error data from a physical address to the corresponding spatial address in the display memory for storage therein.

25. The test circuit of claim 24, further comprising a display coupled to the display memory to display the error data in accordance with the spatial addresses.

26. A testing system for testing a memory device addressable by logical addresses and displaying the locations of errors in the memory device on a display device, the system comprising:

an error memory for storing error data corresponding to a comparison between written and read data to and from the memory device, each memory cell of the catch memory being addressable by a physical address; and

a topological circuit coupled to the error memory and adapted to receive spatial addresses, converting the spatial addresses to selected physical addresses, and providing error data corresponding to the selected physical addresses in response to the spatial addresses to allow the error data from the memory device to map to spatial addresses on the display device to display the locations of errors in the memory device.

27. The testing system of claim **26**, further comprising a programmable router circuit coupled to the error memory to convert the logical addresses to physical addresses, and to route for storage the error data from locations corresponding to the logical addresses within the memory device to memory locations in the error memory corresponding to the physical addresses.

28. The testing system of claim **26** wherein the topological circuit comprises a field programmable gate array.

29. The testing system of claim **26** wherein the topological circuit comprises a read only memory to store a look-up table for converting the spatial addresses to physical addresses.

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